

A Level Detector Design for Dual-Band GSM-PCS Handsets



APN1014

Introduction

Schottky diode detectors are commonly used as amplitude demodulators and level detectors in wireless and other RF and microwave signal processors. Detector designs are simple to realize using low cost, plastic packaged, silicon Schottky diodes. Figure 1 shows a simple conceptual design.

In this application note we will review detector fundamentals and show the performance of a broadband detector that terminates a 50 Ω transmission line. Finally, a design for a level detector is presented for use in a dual band GSM-PCS handset. This application uses Alpha's SMS7630 Zero Bias Detector (ZBD) Schottky diode.

Schottky Detector Fundamentals

Schottky Equation

Schottky diode detector operation is based on the equation that characterizes the current-voltage relationship in a diode junction, as shown:

$$I = I_{SAT} \left(e^{\frac{q(V - IR_S)}{nKt}} - 1 \right)$$

Where: n = ideality factor (typically 1.0)

K = Boltzmann's constant, 1.38044 X10⁻²³ (joule/Kelvin)

q = electronic charge, 1.60206X10⁻¹⁹ (coulombs)

t = temperature (Kelvin)

R_S = series resistance (Ω)

I_{SAT} = saturation current

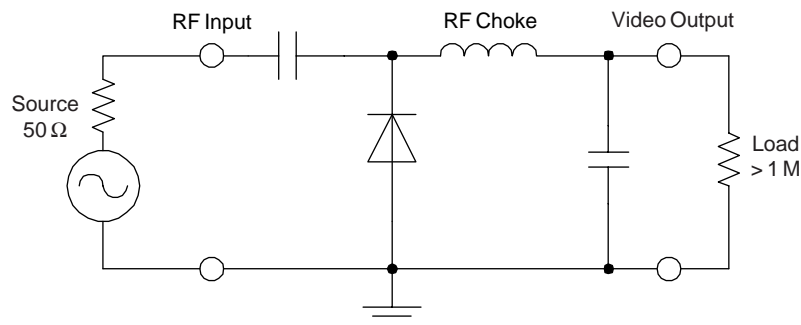


Figure 1. Conceptual Video Detector Circuit

This equation may be simplified for a Schottky diode operated as a zero biased detector at 300 K, where R_S may be neglected and $n = 1.0$ to:

$$I = I_{SAT} (e^{38.6 V} - 1)$$

This equation is appropriate for all junction diodes (PN, PIN and Schottky). However, only for the Schottky diode is this equation valid at high microwave frequencies — even beyond 100 GHz. The Schottky diode employs a metal to semiconductor junction (palladium-silicide on P-type silicon for a ZBD). It is a majority carrier diode with virtually zero minority carrier lifetime (stored charge) to inhibit high frequency performance. PN and PIN junction diodes have finite minority carrier lifetime precluding their use as a detector (or mixer) element at microwave frequencies.

The dynamic resistance of a Schottky diode (the slope of the I-V characteristic) is a function of forward current and may be expressed as:

$$R_V = \frac{nKt}{q} \times \frac{1}{I}$$

This expression also gives the video resistance of the diode at zero bias as:

$$R_V = \frac{0.026n}{I_{SAT}}$$

The video resistance value may then be calculated directly from saturation current.

As a detector, the Schottky diode's performance has been analyzed by simulating the application of a sinusoidal signal at a DC operating point and deriving the generated non-sinusoidal response. Because of the non-linear nature of the diode equation, this response is not sinusoidal but is rich in harmonics. Among the second order terms is a DC component, which is a measure of the magnitude of the applied signal and becomes the generated detector signal.

Square Law and Linear Response

The response of a Schottky detector is generally presented as a curve of detected output voltage vs. applied input power in a circuit where the detector diode terminates a transmission line as shown in Figure 1. At small signals the output voltage is closely proportional to the input power or the square of the input voltage. This is called the square law region. In this region, a 10 dB increase in input power results in a 10 times increase in output voltage. At large input signals the detector voltage is more directly proportional to the input RF voltage. This is the linear region and it is where a 10 dB increase in input power results in a 5 times increase in output voltage. Figure 2 demonstrates this effect.

In a typical level detector, where the video load impedance is much higher than the video resistance of the Schottky diode, the square law region occurs when the output voltage is less than 10 mV. The linear region begins at about 100 mV output voltage. It is more accurate to describe the borders of these regions based on output voltage rather than input power. Output voltage is independent of matching, coupling and source impedance.

The Zero Bias Detector (ZBD)

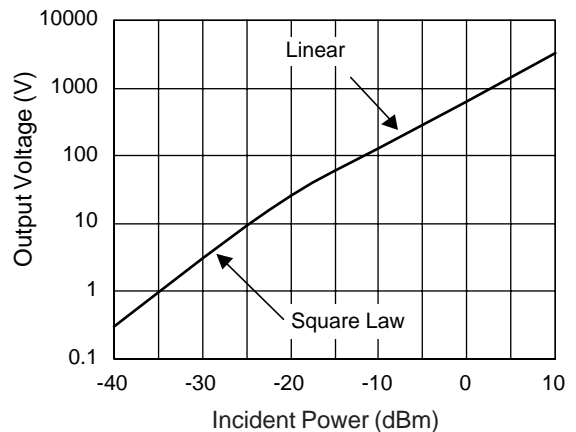


Figure 2. Square Law and Linear Regions

Silicon Schottky diodes are distinguished by their barrier height and are determined by the different metals used in forming the metal-semiconductor junction. Silicon Schottky diodes are available in ZBD, low, medium, and high barrier designs. The primary electrical differences, for the same junction area (capacitance), is the higher the barrier the higher the forward voltage. For Schottky diodes used as mixers the performance benefit of the higher barrier diode is wider dynamic range (lower distortion). Consequently, a higher barrier diode requires higher local oscillator power.

All Schottky diodes operating at zero external bias generate virtually the same open circuit detector voltage at the same input power. In this respect, all Schottky diodes may be considered zero bias detectors. However, the SMS7630 ZBD at zero bias has a video resistance value of typically 3500 Ω. At zero bias the video resistance for the SMS7621, a low barrier Schottky diode with similar capacitance, is about 650 kΩ. In many applications, the video load resistance presented by an operational amplifier is 100 kΩ or less. In this configuration, system sensitivity using the SMS7630 ZBD is significantly better.

Detector Performance

The SMS7630-079 diode has been evaluated in the detector circuit shown in Figure 3 with the Schottky diode terminating a 50 Ω line. Data were taken from 100 MHz to 10 GHz at power levels from -30 dBm to +15 dBm. The SC-79 packaged diode was attached to the terminal of a 3.5 mm connector and the output voltage was measured through a HP11612A bias TEE on a voltmeter with 10 MΩ input resistance.

The results in Figure 3 show that, with no attempt at matching, this low cost device gives a flat response generating approximately 30 mV at -20 dBm across this wide frequency band. The voltage peak at 5 GHz is due to a resonance of the SC-79 package inductance with the diode junction capacitance. This results in higher RF voltage across the diode junction.

Improved detector sensitivity may be achieved by maximizing the RF voltage on the diode junction. This is accomplished by increasing the source impedance. For the SMS7630 with 500 Ω source impedance at -20 dBm input power, the output voltage will be about 130 mV, which is more than 4 times higher than with a 50 Ω source impedance. This type of matching is not the same as the traditional conjugate power match and a consequence of high detector sensitivity is high SWR.

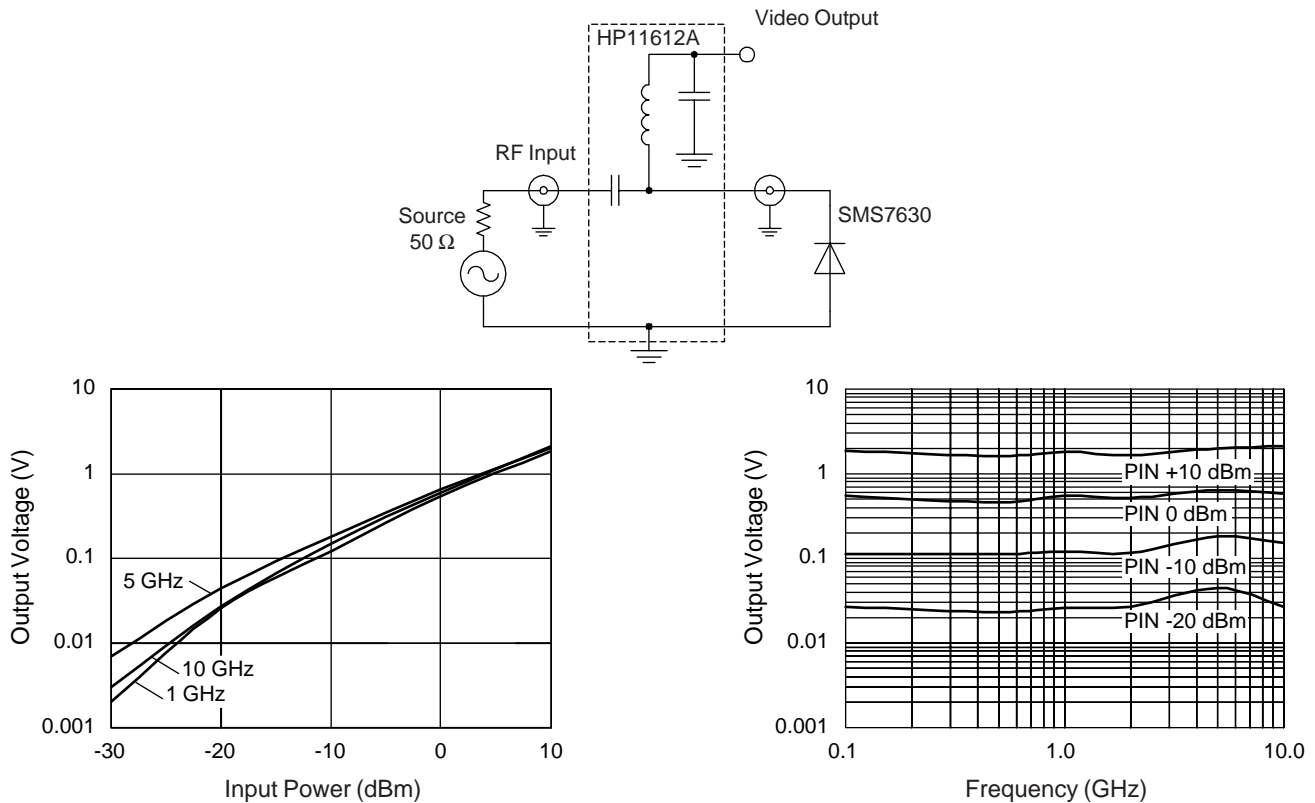


Figure 3. Unmatched Detector and Measurements

Schottky Diode Model

The SPICE model is a reliable representation of the Schottky diode. For the SMS7630, the SPICE model parameters are presented in Table 1.

Parameter	Description	Unit	SMS7630 & Default	SMS1546 & Default
IS	Saturation current	A	5E-6	3E-7
RS	Series resistance	Ω	30	4
N	Emission coefficient (Not used)	-	1.05	1.04
TT	Transit time (Not used)	S	1E-11	1E-11
CJO	Zero-bias junction capacitance (Not used)	F	1.4E-13	3.8E-13
VJ	Junction potential (Not used)	V	0.34	0.51
M	Grading coefficient (Not used)	-	0.4	0.36
EG	Energy gap (with XTI, helps define the dependence of IS on temperature)	EV	0.69	0.69
XTI	Saturation current temperature exponent (with EG, helps define the dependence of IS on temperature)	-	2	2
KF	Flicker-noise coefficient (Not used)	-	0	0
AF	Flicker-noise exponent (Not used)	-	1	1
FC	Forward-bias depletion capacitance coefficient (Not used)	-	0.5	0.5
BV	Reverse breakdown voltage (Not used)	V	2	2.5
IBV	Current at reverse breakdown voltage (Not used)	A	1e-4	1e-5
ISR	Recombination current parameter (Not used)	A	0	0
NR	Emission coefficient for ISR (Not used)	-	2	2
IKF	High-injection knee current (Not used)	A	Infinity	Infinity
NBV	Reverse breakdown ideality factor (Not used)	-	1	1
IBVL	Low-level reverse breakdown knee current (Not used)	A	0	0
NBVL	Low-level reverse breakdown ideality factor (Not used)	-	1	1
TNOM	Nominal ambient temperature at which these model parameters were derived	$^{\circ}\text{C}$	27	27
FFE	Flicker-noise frequency exponent (Not used)		1	1

Table 1. Silicon PN Diode Values in Libra IV Assumed for SMS7630 and SMS1546 Models

The power response at 1 GHz was modeled using these SPICE parameters in a Libra IV platform and using the methodology in Reference 1 showing good compliance of both methods to measured values. This is shown in Figure 4.

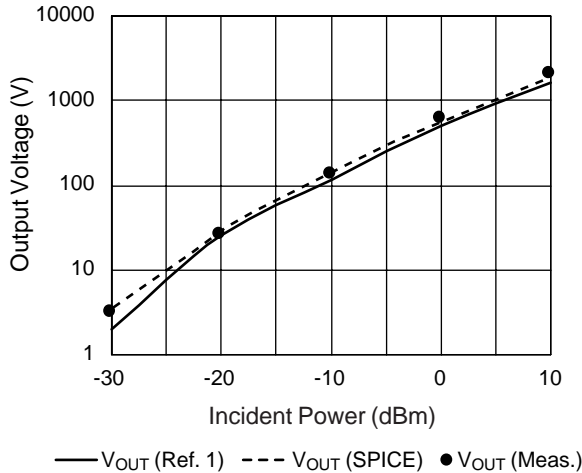


Figure 4. Detector Output Voltage

Dual-Band GSM-PCS Level Detector Design

A detector design was initiated to generate approximately 10 mV at +10 dBm input power using a low loss coupled structure for use as a level detector. The frequency coverage would encompass the GSM and PCS bands for typical usage in a dual-band handset.

Figure 5 shows the design that uses two Schottky diodes in a voltage doubler configuration. In the voltage doubler, the RF voltage is applied to the parallel connection of two diodes, each diode generating the same rectified voltage. The video output is extracted from the series connection of the two diodes thus its magnitude is twice that of a single diode.

The consequence of this design is twice the video resistance, R_v , in comparison to a single diode detector. This does not detract from the performance because the R_v value for a single ZBD Schottky diode is about 5 k Ω — much lower than the input impedance of the typical operational amplifier following the detector. Higher order voltage multipliers may be designed using the same principle.

In the Libra IV model shown in Figure 6, the SMS7630-079 Schottky diodes DIOD1 and DIOD2 are used in a voltage doubler configuration. Capacitors C_4 and C_5 , and inductors L_1 and L_2 simulate the effect of the SC79 package. Capacitor C_2 reflects the mounting pad capacitance. The RF coupling is realized through a high impedance resistive voltage divider, consisting of two resistors.

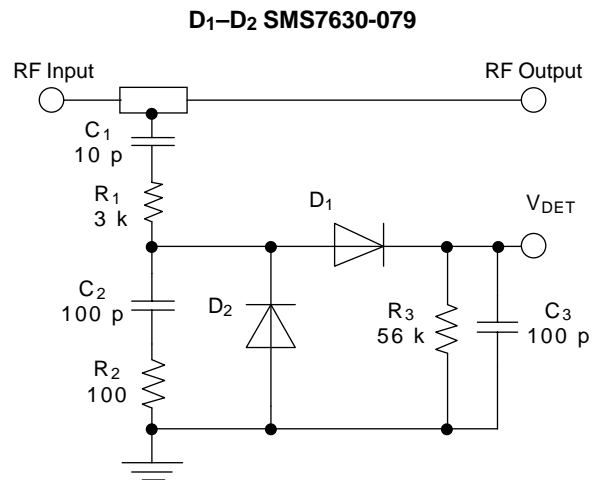


Figure 5. Level Detector Circuit Diagram

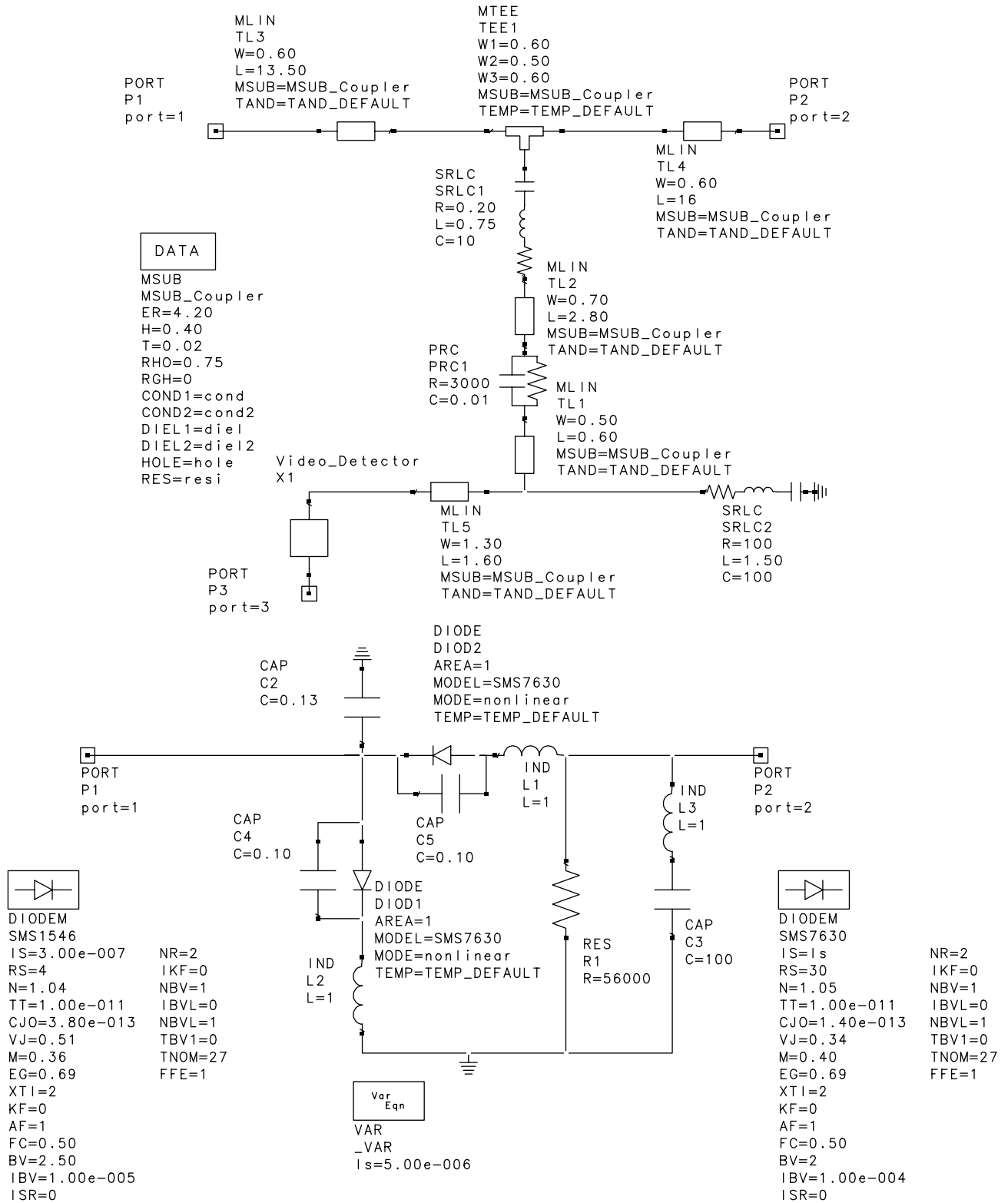


Figure 6. Level Detector Circuit Model

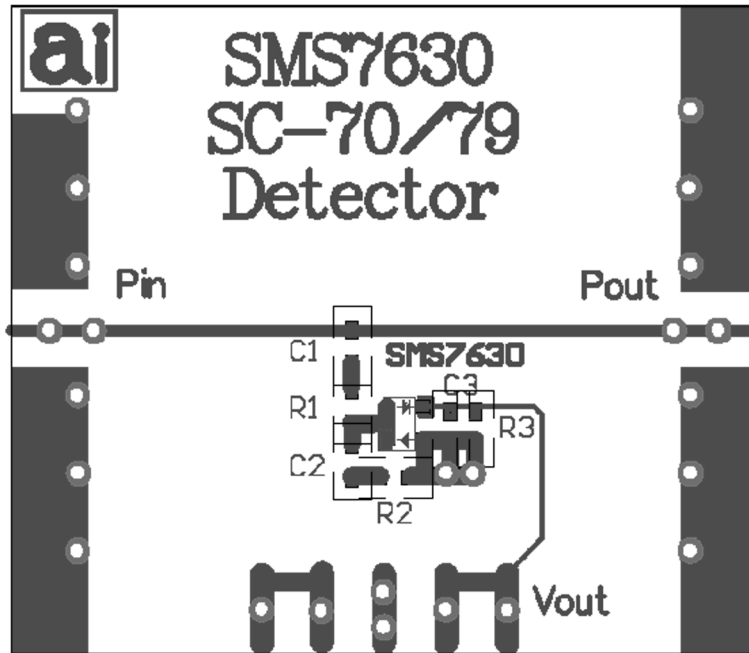


Figure 7. Detector PCB Layout

PRC1 = 3 kΩ and SRLC2 = 100 Ω. The total impedance of the divider is 3500 Ω causing about a 0.06 dB loss in the transmission path from Port 1 to Port 2. Capacitors SRLC1 and SRLC2 are used to prevent DC current leakage.

The PCB layout is shown in Figure 7, and the Bill of Materials is shown in Table 2.

Designator	Value	Part Number	Footprint	Manufacturer
C ₁	10 p	CM05CG100K10AB	0402	AVX
C ₂	100 p	CM05CG5101K10AB	0402	AVX
C ₃	100 p	CM05CG5101K10AB	0402	AVX
R ₁	3 k	CR05-302J-T	0402	AVX/KYOCERA
R ₂	100	CR05-101J-T	0402	AVX/KYOCERA
R ₃	56 k	CR05-563J-T	0402	AVX/KYOCERA
D ₁	SMS7630-079	SMS7630-079	SC-79	ALPHA IND.
D ₂	SMS7630-079	SMS7630-079	SC-79	ALPHA IND.

Table 2. Bill of Materials

Dual-Band Detector Performance

In Figure 8, the measured detector DC output voltage is shown vs. input power in the through-line at 1 GHz simulating the GSM band and at 2 GHz simulating the PCS band. Both measured and simulated results agree. A useful dynamic range of 32 dB is achieved based on an output voltage range from 10 mV to 2 V.

The coupling ratio of this detector circuit is about 37 dB in a 50 Ω environment. This circuit may be modified by changing the through-line resistors R₁ and R₂. This allows the designer to achieve the same output voltage

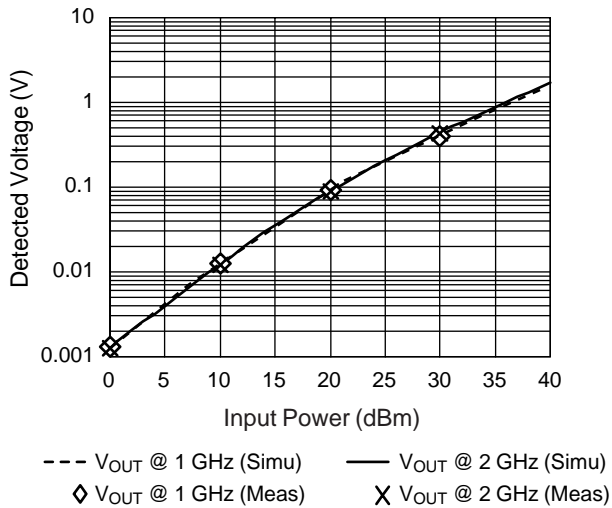


Figure 8. Detector Output Voltage vs. Input Power

Input Power	V _{OUT} mV	V _{OUT} mV	V _{OUT} mV	V _{OUT} mV	V _{OUT} mV	V _{OUT} mV
	800 MHz	1 GHz	1.2 GHz	1.8 GHz	2.0 GHz	2.2 GHz
-10 dBm	0.131	0.129	0.128	0.122	0.118	0.112
0 dBm	1.24	1.23	1.22	1.21	1.18	1.13
5 dBm	4.15	4.13	4.11	3.88	3.84	3.12
10 dBm	12.23	12.21	11.99	11.91	11.53	11.39
15 dBm	34.81	34.62	34.33	33.77	33.65	33.53
20 dBm	91.38	91.36	91.35	88.86	86.51	83.91
30 dBm	422.65	422.61	422.15	421.38	419.38	405.31

Table 3. Detector Frequency Response

performance at different input power levels. Table 3 demonstrates the flatness of the frequency response at different signal levels.

In the 800 MHz to 1 GHz band the detector was flat within 0.10 dB; between 1.8 GHz and 2 GHz flatness was better than 0.15 dB.

The through-line insertion loss of the detector is less than 0.3 dB at frequencies below 1 GHz and less than 0.4 dB in the band between 1.8 GHz and 2.0 GHz. Figure 9 shows that this difference agrees well with the loss model used in the simulation.

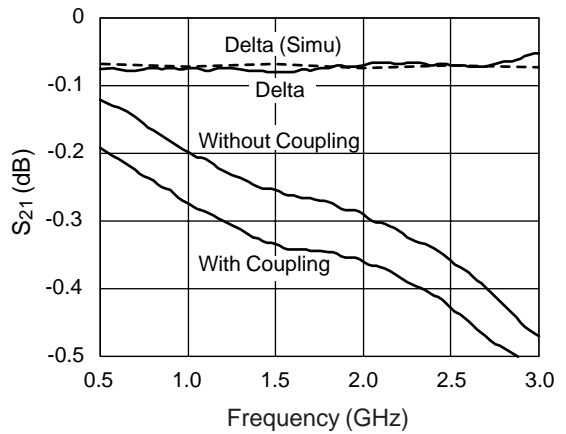


Figure 9. Detector Loss vs. Frequency

Conclusion

This application note demonstrates a detector design that may be used for level setting in a dual-band handset. It operates with frequency flatness better than 0.15 dB in any band. The design utilizes two low cost, plastic packaged Alpha SMS7630-079 ZBD Schottky diodes in a voltage doubler. Although intended for GSM-PCS service, the design is appropriate for any dual-band applications covering 800 MHz to 2.4 GHz.

References

R.G. Harrison, X. LePolozec, "Nonsquarelaw Behavior of Diode Detectors Analyzed by the Ritz-Galerkin Method," *IEEE Trans. Microwave Theory*, May 1994.

List of Available Documents

The Level Detector Simulation Project Files for Libra IV.

The Level Detector PCB Gerber Photo-plot files.